

# Radiation Performance of 1 Gbit DDR SDRAMs Fabricated in the 90 nm CMOS Technology Node

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**Abstract**— We present Single Event Effect (SEE) and Total Ionizing Dose (TID) data for 1 Gbit DDR SDRAMs (90 nm CMOS technology) as well as comparing this data with earlier technology nodes from the same manufacturer.

**Index Terms**—radiation effects, reliability estimation, quality assurance

## I. INTRODUCTION

Synchronous Dynamic Random Access Memories (SDRAMs) are both a cutting edge CMOS technology and an enabling technology for space flight. As such, radiation test results are of interest to both technologists and designers. Single event latchup (SEL) response is a major concern, since it has made recent commercial memory generations difficult and expensive to qualify. This is because even for parts that remain functional after SEL, reliability may be compromised by latent damage.[1] In this poster, we present data on the Single-Event Effects (SEE) and Total Ionizing Dose (TID) susceptibility of Samsung 1 Gbit Double Data Rate (DDR) SDRAMs (K4H1G0438—see figure 1).[2]

Devices Tested: Samsung K4H1G0438

256M x 4 configuration

66-pin Thin Shrink Small Outline Package (TSSOP)

Internal speeds up to 266 MHz

Vdd: 2.5 V

Die Revisions (Revs):

NASA GSFC: Rev A (90 nm CMOS)

The Aerospace Corporation: Rev M (100 nm CMOS)

Test Systems:

NASA GSFC's Low-Cost Digital Tester (LCDT—see figure 1) and Aerospace's test system have been described previously.[3, 4]

### A. Test Facilities – Heavy Ion

NASA GSFC performed tests at:

- SEE Test Facility (SEETF) at Michigan State University (high Linear Energy Transfer—LET) .[5]
- -Texas A&M University Cyclotron Center (TAMU – The 40 MeV/amu tune was used to ensure penetration to the sensitive volume from the front-side for low LET ions.)

The Aerospace Corporation used the Lawrence Berkeley National Laboratory's (LBNL) 88-inch Cyclotron.

TABLE I: EFFECTIVE LET OF TEST IONS

Ion/ Energy	Energy/ amu	Angle	Facility	Effective LET	Residual Range
Xe-136	69.9	0°	NSCL	27	640 $\mu\text{m}$
Xe-136	69.9	45°	NSCL	46.5	182 $\mu\text{m}$
Xe-136	69.9	60°	NSCL	107.6	123 $\mu\text{m}$
Ne-20	40	0°	TAMU	1.4	1.1 mm
Ar-40	40	0°	TAMU	5.8	420 $\mu\text{m}$
B-10	10	0°	LBNL	1	225 $\mu\text{m}$
O-16	10	0°	LBNL	2.4	165 $\mu\text{m}$
Ne-20	10	0°	LBNL	4	117 $\mu\text{m}$
Ar-20	10	0°	LBNL	14	51 $\mu\text{m}$
Cu	10	0°	LBNL	33	29 $\mu\text{m}$
Kr	10	0°	LBNL	41	38 $\mu\text{m}$
Xe-136	10	0°	LBNL	59	30 $\mu\text{m}$

### B. Test Facilities - Proton

The Aerospace Corporation used LBNL as well as the Indiana University Cyclotron Facility (IUCF). Proton energies at LBNL were 20, 30 and 50 MeV, while those at IUCF were

Manuscript received July 8, 2006. The authors would like to thank NASA's Electronic Parts and Packaging (NEPP) program and the Defense Threat Reduction Agency IACRO 06-4012I for support of this research.

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98 and 200 MeV. All proton testing was done at normal incidence.

## II. HEAVY-ION SEE TESTING

### NASA GSFC

Initial SEE testing was carried out at the SEETF on packaged devices. Due to temporal and economical constraints, testing was conducted with a single ion incident at  $0^\circ$ ,  $45^\circ$ , and  $60^\circ$  to the DUT normal to give 3 effective LETs. Effective LET in the active volume was calculated based on the energy lost by the ion beam as it traversed the layers over the sensitive volume (e.g. plastic molding, lead frame, etc.) [6] (See figure 2, for example.) Lead frame and package composition and thickness were derived from information supplied by the vendor.

An attempt was made to repackage several of the TSSOP DUTs to allow easier characterization at TAMU. This repackaging was unsuccessful (timing/signal drive issues), and the higher energy (40 MeV/amu) tune was used to characterize the DUT in the low LET range. To ensure that ion LET could be determined unambiguously, only data for normal incidence ions are reported here. LET for the tests at TAMU was estimated using the same method as was used for the SEETF.

### The Aerospace Corporation

Heavy-ion testing at the LBNL facility used a 10 MeV/amu tune, so the DUTs were thinned to a thickness of 3 mils (about  $76.2\ \mu\text{m}$ ) and mounted face down so they could be irradiated from the backside. All ions were incident normal to the device.

### Test Methods

Both NASA GSFC and The Aerospace Corporation used similar testing methods. The test flow was as follows:

- Write DUT with a fixed test pattern
- Read back test pattern and verify.
- Begin Irradiation and read DUTs repeatedly
- If a reading differs from the programmed pattern, tally a single-event upset (SEU). Aerospace corrected the error before continuing reading, while GSFC did not.
- If a large number of errors occur simultaneously, and errors continue after the beam was stopped, we stop the run and tally a single-event functional interrupt (SEFI). If errors do not continue with no beam, the large error is tallied as a burst, block or column error.
- A SEFI causing a significant power supply current jump and not recovering after stopping the beam and refreshing device mode registers was called an SEL.

Because of the complexity of SEE data for SDRAMs, the addresses, values and times of all errors were recorded for post processing to extract multi-bit upsets, different SEFI modes, stuck bits, etc. The Aerospace Corporation conducted all irradiations at room temperature. GSFC looked for SEL

susceptibility at both ambient temperature and at  $85^\circ\text{C}$ .

Internal DUT frequencies were 100 MHz.

The Aerospace Corporation performed proton tests at LBNL and IUCF with a primary emphasis on SEE (similar method to heavy ion testing). TID data were taken noting only functional performance and supply current variances. No additional parametric measurements were made during testing.

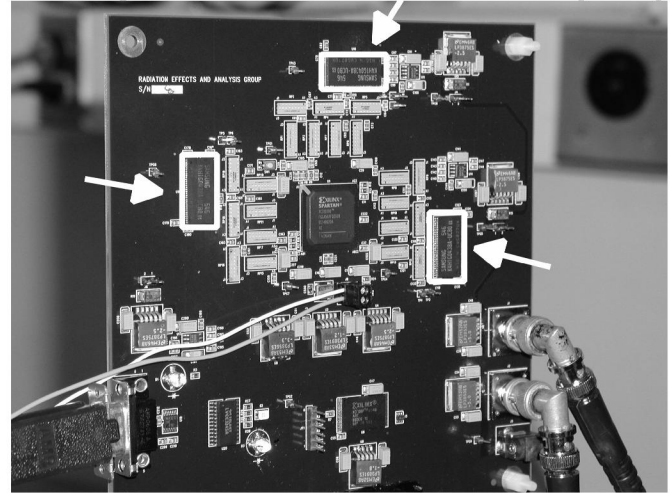


Fig. 1. NASA GSFC's Low-Cost Digital Tester, configured to test high-density DDR SDRAMs. DUTs are indicated by a red dot on the package.

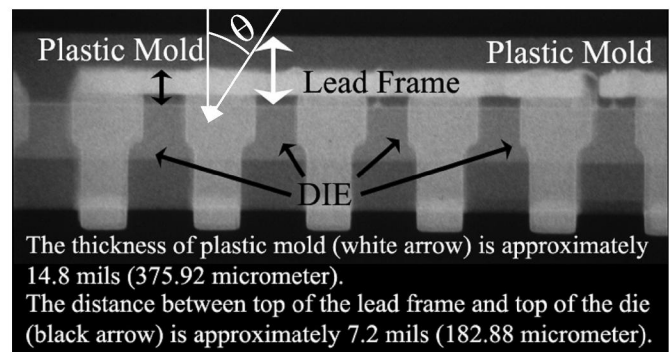


Fig. 2. X-Ray Photo of the DUT. Determining effective LET as a function of angle requires correcting for the energy lost by the ion as it traverses overburden to the sensitive volume, as well as the usual  $1/\cos\theta$  dependence.

## III. DATA ANALYSIS

In terms of error types and complexity, an SDRAM is more like a microcontroller with a large memory array than a simple memory array. Effects of SEFIs are particularly important for most space applications. [4, 7]

The two organizations independently performed data analysis. Though similar methodologies were utilized, SEFI definition and data parsing may have differed. Additionally, the fact that there were two die revisions tested may skew results. No attempt was made to coordinate the analyses.

### GSFC SEE Data Analysis

During post processing, based on the time stamps, addresses and memory contents, data were classified into:

- Single-bit Upsets (SBUs)
- Multi-bit upsets (MBUs)
- Burst errors (temporary strings of errors – self-

- recovering)
- Burst errors (persistent – non-recovering) classified as SEFI
- Address errors (multiple errors in same row, block, or column)
- SEL

Because statistics for the burst error modes and address errors was limited, and because they often have comparable operational consequences, these three modes are combined and reported here as “SEFI” in the results section. Because it can be difficult to determine all the effects of such large errors, SBUs and MBUs were determined using only the portion of each run before such a “SEFI” was observed.

#### The Aerospace Corporation Data Analysis

The Aerospace Heavy ion and proton data were analyzed in a manner similar to GSFC’s. Based on the totals for each error type and the fluence accumulated up to the occurrence of the first SEFI or other large error, average cross sections were calculated for all the runs at each effective LET value. Aerospace observed no multi-bit errors and only one run at the highest LET showed a SEFI. Aerospace observed no multi-bit errors and only runs with  $LET \geq 14$  MeVcm<sup>2</sup>/mg showed SEFIs.

TID data concerned only functionality and consisted of observing that parts remained functional with no gross changes in error rates at the highest test operating speed as dose accumulated during proton testing.

#### IV. HEAVY-ION AND PROTON SEE RESULTS

##### GSFC Results – SEL at NSCL SEETF

SEL was observed only at the highest LET tested (108 MeV\*cm<sup>2</sup>/mg) and at elevated temperature (85 °C). Figure 3 shows the measured SEL cross section and the upper limit for the cross section at the next highest LET tested (47 MeV\*cm<sup>2</sup>/mg). Although we cannot definitely rule out the possibility of SEL between these two LET values, the low SEL cross section at 108 MeV\*cm<sup>2</sup>/mg suggests that the threshold is probably closer to this value rather than the lower limit of the range.

##### GSFC SEE Results

Figure 4 shows cross sections for SBU, MBU and SEFIs (determined in post processing) as a function of effective LET. It is interesting to note that the MBU cross section (for >1 bit upset) is nearly a constant proportion of the SEU cross section over the high-LET range carried out at the MSU SEETF. Both the SEU and MBU cross section continue to increase up to the highest effective LET tested, while the SEFI cross section appears to saturate over this range. MBUs and “SEFIs” were only observed in the SEETF data ( $LET > 27$  MeVcm<sup>2</sup>/mg).

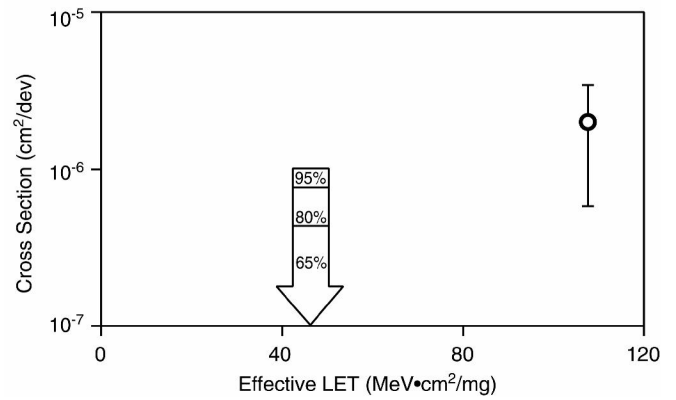


Fig. 3. SEL cross section and upper limits thereof as a function of effective LET.

#### Aerospace Results

Figure 5 shows The Aerospace Corporation heavy-ion SEU data from LBNL. The bit-error cross section is approximately 20x higher than the cross section for single-bit errors for the GSFC data on the rev. A die. No MBUs were noted in this data. SEFIs were seen only at  $LET \geq 14$  MeVcm<sup>2</sup>/mg (open triangles in figure 5). At least two “SEFI” modes were observed. One mode would be better characterized as a burst error, in which a large number of errors are seen, but recovery can be achieved by simply rewriting the data into the memory. The other mode is properly a SEFI, as power cycling was necessary to recover normal device functionality. No SEL was seen at room temperature. The upper bound of the 95% confidence level (CL) for SEL cross section is  $10^{-6}$  cm<sup>2</sup>.

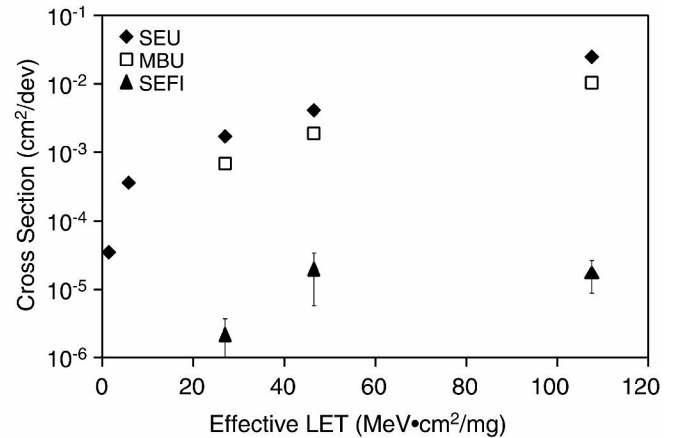


Fig. 4. SEU, MBU and SEFI cross sections as a function of effective LET for GSFC data (statistical error bars shown if they are not negligible).

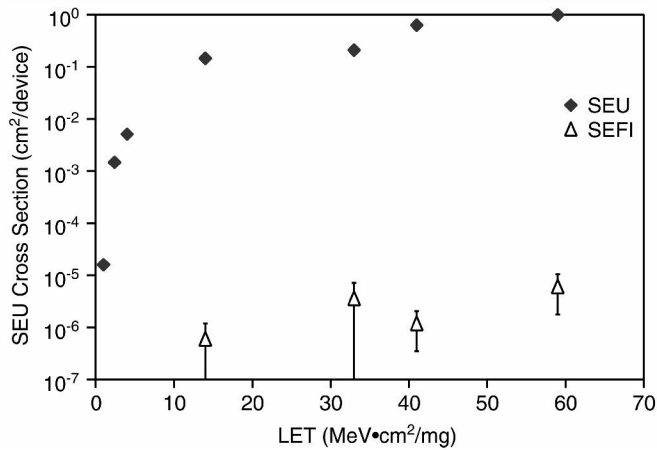


Fig 5. Cross section vs. LET for heavy ions from data taken by the Aerospace Corporation.

Multiple potential explanations exist on the differences between the GSFC and The Aerospace Corporation's results. They include:

- Different die revisions (A versus M)
- Different test ion energy/particle ranges (NSCL SEETF and TAMU versus LBNL)
- Thinned die versus unmodified
- Angular effects versus normal incidence

Figure 6 shows The Aerospace Corporation's proton SEU data for both the 1 Gbit DDR and the preceding generation 512 Mbit DDR from the same vendor. As expected due to geometric cell size issues, the per bit cross sections for the 1 Gbit device are somewhat lower than for the 512 Mbit DDR. All errors observed were isolated single-bit errors—which is not unexpected since all runs were performed with the proton beam incident normal to the device.

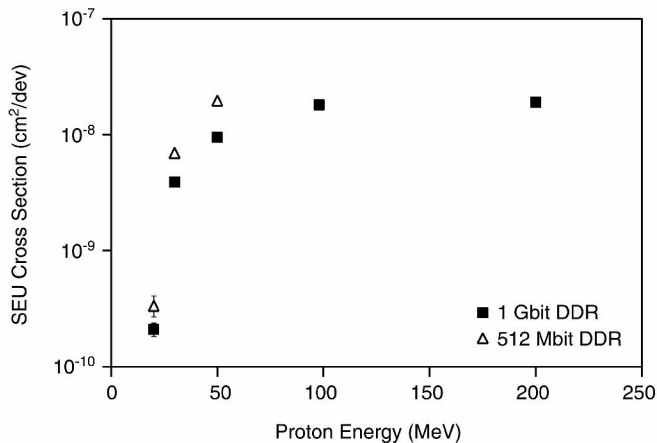


Fig. 6. SEU cross section vs. proton energy. Statistical error bars are shown if they are not negligible.

## V. TID DEGRADATION

TID degradation is generally thought to improve as CMOS feature size shrinks. However, the very stringent requirements on leakage currents in DRAM access FETs make this more uncertain for DRAMs. While detailed studies of TID induced parametric degradation remain to be done, the parts tested

with protons by Aerospace functioned with no apparent degradation to >100 krad(Si).

## VI. FUTURE WORK

While the test results to date are encouraging for use of these memories in space missions, several hurdles remain to be traversed. Full parametric TID testing is scheduled to be performed once additional test parts are received in August. Proton testing over angles is also anticipated to better characterize susceptibility to multi-bit SEU and other proton-induced effects. We also plan to extend our study of volatile memory devices as parts from other vendors and new generations of technology become available.

## VII. DISCUSSION

Data for the current 1 Gbit 90 nm feature size DDR SDRAMs demonstrate that reduced feature size does not necessarily correlate to worse radiation performance. SEU cross sections on a per bit basis are lower than those of the previous 512 Mbit devices. SEL performance of the 1 Gbit devices is significantly better than for previous generations (see Table II), and SEU, MBU and SEFI rates remain manageable with mitigation techniques used with previous generations (error correction codes, error scrubbing, creative memory organization and so on.). For example, a conservative fit to the GSFC data yields rates for Geostationary orbit of 10<sup>-11</sup>-10<sup>-10</sup> upsets per bit per day for the revision A die, while the Aerospace data yield a rate roughly 10 times higher for the revision M die. SEFIs and other block errors can be expected to occur at a rate of roughly 10<sup>-4</sup> per device-day. Multibit upsets could occur at a rate of once in 10-100 days. Protons should not cause either SEFIs or MBUs in the absence of significant angular effects.

The current work also demonstrates that even if a device is not amenable to repackaging or other package modification for SEE testing, high-energy ions (e.g. at MSU's SEETF and at TAMU) can be used to obtain a thorough characterization of the device. In carrying out such a strategy, it is helpful to capitalize on the greater LET selectability at TAMU, making use of the SEETF primarily for high-LET ions that cannot be delivered by lower energy facilities. It is also helpful to have a detailed understanding of the overburden the beam must penetrate above the sensitive volume.

TABLE II: SEL ONSET LETs SDRAM GENERATIONS.

Part # and Size	SEL LETth MeV·cm²/mg	Reference
64 Mbit	Not observed	8
128 Mbit	4.4 < LETth < 15	8
256 Mbit	28 < LETth < 35	8
512 Mbit	30 < LETth < 47.6	9
1 Gbit	46.5 < LETth < 107.6 (85°C)	This Work

## VIII. CONCLUSION

The radiation performance (SEE and TID) of the Samsung

1-Gbit DDR SDRAMs makes them excellent candidates for space flight applications. SEL susceptibility is low, especially at low temperatures. SEFI and block error susceptibility appear to be comparable to that of previous generations. MBUs were seen at high LET in SEE testing of the rev. A version of the die, but not the rev. M version. The Rev. M version also yielded a higher per bit cross section than the rev. A die. Finally, we note that in the past SDRAMs have shown lot-to-lot variation in TID and SEE susceptibility. Additional testing is strongly advised to ensure adequate radiation performance in future applications.

## REFERENCES

- [1] H. N. Becker, "Latent damage in CMOS devices from single-event latchup", IEEE Trans. Nucl. Sci. 49, No. 6, Dec. 2002, 3009 - 3015.
- [2] Version M: [http://www.samsung.com/Products/Semiconductor/DDR\\_DDR2/DDRSDRAM/Component/1Gbit/K4H1G0438M/ds\\_ddr\\_1gb\\_m\\_die\\_x4x8\\_rev10.pdf](http://www.samsung.com/Products/Semiconductor/DDR_DDR2/DDRSDRAM/Component/1Gbit/K4H1G0438M/ds_ddr_1gb_m_die_x4x8_rev10.pdf) , Version A: [http://www.samsung.com/Products/Semiconductor/DDR\\_DDR2/DDRSDRAM/Component/1Gbit/K4H1G0438A/ds\\_k4h1g0x38a\\_rev04.pdf](http://www.samsung.com/Products/Semiconductor/DDR_DDR2/DDRSDRAM/Component/1Gbit/K4H1G0438A/ds_k4h1g0x38a_rev04.pdf)
- [3] J. Howard, "Development of a Low-Cost and High-Speed Single Event Effects Testers based on Reconfigurable Field Programmable Gate Arrays (FPGA)," 2006 Single-Event Effects Symposium, Long Beach, CA, April 10-12, 2006.
- [4] R. Koga et al., "Permanent Single Event Functional Interrupts (SEFIs) in 128- and 256-megabit Synchronous Dynamic Random Access Memories," Radiation Effects Data Workshop, 2001, 16-20 July 2001, 6-13.
- [5] R. Ladbury, "Performance of the high-energy single-event effects test Facility (SEETF) at Michigan State University's National Superconducting Cyclotron laboratory (NSCL)", IEEE Trans. Nucl. Sci. 51, No. 6, Dec. 2004, 3664 - 3668 .
- [6] J. F. Ziegler et al., The Stopping and Range of Ions in Solids. New York: Pergamon, 1984.
- [7] J. Benedetto, "Examination of Single Event Functional Interrupts (SEFIs) in COTS SDRAMs," 2006 Single-Event Effects Symposium, Long Beach, CA, April 10-12, 2006.
- [8] R. Koga et al., "SEE sensitivity determination of high-density DRAMs with limited-range heavy ions," Radiation Effects Data Workshop, 2003. IEEE, July 21-25, 2003, 182-189.
- [9] T. Langley et al., "Single-event Effects Test Results of 512MB SDRAMs," Radiation Effects Data Workshop, 2003. IEEE, July 21-25, 2003, 98-101.